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Question Bank

Linear and Digital integrated circuits (Electronics Paper No.- IV)

MCQ

1. Flip- flop is a ..... circuit

a) Astable b) Monostable

c) Bistable d) Schmitt trigger

2. In a D Flip-flop.....input is called synchronous input of the flip- flop.

a) reset b) preset

c) clear **d) D**

3. Shift register consist of number of …….

a) transistor b) ICs

c) flip-flops d) Latches

4. The IC 7495 is a …….

a) counter **b) up/down counter**

c) decade counter d) shift register

5. The IC.....can be used for synchronous decade counter.

a) 7492 b) 7493

c) 7490 d) 7491

6. R-2R ladder network is used for..... conversion.

a) analog to digital **b) digital to analog**

c) digital to parallel d) all of these

7. Successive approximation method is used for……

a) ADC b) DAC

c) AAC d) DDC

8. An ideal Op-amp has.....input impedance.

a) 0Ω b) 75Ω

c) 2MΩ **d) infinite Ω**

9. For an idea Op-amp, the slew rate is ……..

a) **infinite** b) zero

c) 0.5V/μs d) 0.5V/μs

10. The gain in a Wien Bridge element is a ……

a) 29 b) > 29

c) 3 d) 19

11. The preset and clear are …… inputs in the flip- flops.

a) Synchronous **b) asynchronous**

c) control d) none of these

12. The integrator work well at ..... frequency.

a) high b) low

c) medium d) none of these

13..... pin of IC 555 is a reset pin.

a) 2 **b) 4**

c) 3 d) 7

14) In R-S flip-flop if R=S=1, then this state is called as..... state.

a) set **b) forbidden**

c) reset d) toggle

15) The Master Slave J-K flip- flop avoids.....condition.

a) racing b) **race around**

c) toggle d) last state

16) ..... Clock pulses are required to shift the 4 bit data in SISO shift register.

a) 4 b) 8

c) 6 d) 3

17) The IC 74190 can be used as ..... shift register.

a) 3 bit b) bidirectional

c) 4- bit d) none of these

18) The 3- bit binary ripple counter counts the maximum.....states.

a) 4 b) 6

c) 9 **d) 8**

19) Asynchronous counter is also called.....Counter.

a) combinational **b) ripple**

c) parallel d) down

20) The counter is a..... type of logic circuit.

a) analog b) sequential

c) combinational d) none of these

21) The preset and clear are .... inputs in the flip-flops.

(a) synchronous **(b) asynchronous**

(c) control (d) none of these

22) 6. In J-K flip-flop, when J = 1 and K = 1, it is possible to.....the flip-flop.

(a) set (b) reset **(c) toggle** (d) none of these

23) …… flip-flop is used to avoid race-around condition.

(a) JK M/S (b) RS (c) JK (d) none of these

24) A single J-K flip-flop connected in toggle mode, it works as a divide by……device.

(a) 4 **(b) 2** (c) 6 (d) 8

25) In… ..... shift register, the data has maximum speed.

(a) serial in-serial out (b) serial in-parallel out
(c) parallel in-parallel out (d) parallel in-serial out

26) The shift registers are used for.....data.

(a) shifting (b) subtracting (c) adding (d) none of these

27) In shift register, each bit is shifted on a……

(a) clock transition (b) input signal (c) output signal (d) source voltage

28) The IC…… is a 4-bit binary ripple type divide-by-twelve counter.

(a) 7492 (b) 7493 (**c) 7490** (d) 7491

29) The logic circuit used to count the number of pulses is called… ..... circuit.

(a) flip-flop **(b) counter** (c) register (d)none of these

30) DAC 0808 is ..... bit D to A converter.

a)16 b)4 c)32 **d)8**

31) ADC 0804 is ..... bit ADC.

(a) 4 (b) 8 (c) 32 **(d) 16**

32) DAC 0808 is ..... pin IC.

(a) 8 **(b) 16** (c) 20 (d) 24

33) The differentiating circuit works well when the signal frequency is…….

(a) high **(b) low**

(c) medium (d) none of these

34) In dual slope conversion method, conversion time is
(a) very small (b)large (c) zero (d) very large

35) In an integrator, the feedback element is a……

(a) resistor **(b) capacitor**

(c) diode (d) zener diode

36) Zero-level detector is one application of a

(a) diode (b) differentiator

(c) comparator (d) integrator

37) The Wien Bridge oscillator is useful

(a) At high frequencies **(b) At low frequencies**

(c) At small input signal (d) In LC circuit

38) An ideal Op-Amp has……output impedance.
(**a) 0 Ω** (b)2M Ω (c) 75 Ω (d) infinite Ω

39) Op-Amp is basically……..

(a) DC amplifier (b) RC coupled amplifier

(c) differential amplifier (d) none of these

40) The parameter which decides the speed of Op-Amp is....

(a) SVRR (b) CMRR **(c) slew rate** (d) UGB

41) An astable multivibrator has stable state.

(a) one (b) two **(c) no** (d) one quasi

42) In IC 555 timer, the pin number 7 stands for.....

(a) threshold (b) reset (c) trigger **(d) discharge**

Q2) Attempt any two of the following: (10 marks each) **[20]**

a) Explain Op-Amp as inverting and non- inverting amplifier.

b) Explain the functional block diagram of IC 555.

c) With proper circuit diagram, explain in detail R-2R ladder method of DAC.

d) Explain the working of RS flip- flop using transistor with truth table.

e) Describe the working of JK flip-flop with logic diagram and truth table

f) Explain the brief 4- bit left shift and right shift register with proper diagram.

Q3) Attempt any four of the following: (5 marks each) **[20]**

a) Explain the working of RS flip- flop using NOR gate.

b) Explain the working of D flip- flop and state its advantages.

c) Draw the logic diagram of SIPO shift register and explain it.

d) Explain 4 –bit ring counter.

e) Explain the up/ down counter.

f) Explain the frequency response of Op- Amp.

g) What is an Op-Amp? Give its schematic symbol and its equivalent circuit.

h) 7. Define the following parameters:

(a) Input offset current, (b) Input offset voltage, (c) Input bias current.

i) List the features of ADC 0804.

j) Explain in short successive approximation method of ADC.

k) Define the terms:

(a) Accuracy, (b) Resolution, (c) Settling time.

l) Explain the working of D flip- flop and state its advantages.

m) Explain 4 –bit asynchronous binary counter.

n) Explain the JK flip flop.

o) Explain preset and clear facilities in D flip-flop, draw its logic diagram.

p) Explain the frequency response of Op- Amp.

q) Explain the working of RS flip- flop using NAND gate.

r) What is meant by shift register? Give types of shift register.

s) Draw the logic diagram of PIPO shift register and explain it